ABSTRACT OF THE DISCLOSURE

A hierarchically organized, compilable semiconductor memory circuit having multiple levels with simultaneous access and cache loading. A first level memory portion and at least a next level memory portion are provided as part of the semiconductor memory circuit, wherein the memory portions are associated with separate Data In (DIN) and Data Out (DOUT) buffer blocks for effectuating data operations. DIN buffer blocks of the first level and intermediate levels, if any, are provided with multiplexing circuitry that is selectively actuatable for providing data accessed in the next level memory portion to Local Data In (LDIN) driver circuitry, whereby the accessed data is simultaneously loaded into the first and intermediate levels. Accordingly, extra clock cycles are saved from cache loading of the data used for subsequent memory operations.